Testbench

module Slave\_TB ();

reg clk;

wire SDA;

wire SCL;

pullup(SDA);

pullup(SCL);

reg [6:0] addressToSend = 7'b000\_1000;

reg readWite = 1'b1;

reg [7:0] dataToSend = 8'b0110\_0111;

integer ii=0;

initial begin

clk = 0;

force SCL = clk;

forever begin

clk = #1 ~clk;

force SCL = clk;

end

end

Slave #() UUT

(.SDA(SDA),

.SCL(SCL));

initial

begin

$display("Starting Testbench...");

clk = 0;

force SCL = clk;

#11

// Set SDA Low to start

force SDA = 0;

for(ii=0; ii<7; ii=ii+1)

begin

$display("Address SDA %h to %h", SDA, addressToSend[ii]);

#2 force SDA = addressToSend[ii];

end

$display("Read/Write %h SDA: %h", readWite, SDA);

#2 force SDA = readWite;

release SDA;

$display("SDA: %h", SDA);

#2; // Wait for ACK bit

for(ii=0; ii<8; ii=ii+1)

begin

$display("Data SDA %h to %h", SDA, dataToSend[ii]);

#2 force SDA = dataToSend[ii];

end

#2;

release SDA;

#2 force SDA = 1;

#100;

$finish();

end

initial

begin

$dumpfile("dump.vcd");

$dumpvars(0);

end

endmodule